DETAILED ACTION

Response to Amendment

1. This action is responsive to amendments filed on 4/13/2011.

2. Claims 1-17 and 32 are presented for examination.

3. Claims 18-29 are withdrawn and Claims 30-31 are cancelled.

4. Applicant's amendments to the abstract have been considered and the spec objections have been withdrawn.

5. Applicant's amendments to the claims have been considered and the claim objections have been withdrawn. Current claim objections pertain to the new claim amendments.

6. Applicant's amendments to the claims have been considered and the rejections under 35 USC 112 have been withdrawn.

Claim Objections

7. Claim 1 is objected to because of the following informalities: The claim recites in last line of page 3 of the claims "CAM and RAM memory portions", the acronyms 'CAM and RAM' should be spelled out in at least the first time the terms are mentioned in the claim. For instance, the claim should be amended as follows –content addressable memory (CAM) and random access memory (RAM)-- Appropriate correction is required.

8. Claim 5 is objected to because of the following informalities: The claim recites "The data processing device as defined in claim 4", claim 4 is cancelled. Appropriate correction is required.

9. Claim 5 also recites "(5) when an address of the register and/or the main memory means" (see last limitation of page 8 of the claims), there is a lack of antecedent basis for the 'main memory means' in the claims. Appropriate correction is required.

10. Claims 6 and 7 are objected to because of the following informalities: The claims recite "The data processing device as defined in claim 4", claim 4 is cancelled. Appropriate correction is required.

11. Claim 9 is objected to because of the following informalities: The claim recites "a temporal storage section which stores a indication of a change", it should be changed to --a temporal storage section which stores **an** indication of a change-- Appropriate correction is required.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable Sodani et al. U.S. Patent No. 5,845,103 (hereinafter Sodani) in view of Crick et al. U.S. Patent No. 5,285,527 (hereinafter Crick).

14. As per claim 32, Sodani teaches a data processing apparatus for speeding-up execution of program instructions read from a main memory, comprising:

a main memory which stores program instructions (see Fig. 1, element 12);

at least one instruction stream processor (Fig. 1, element 10) comprising:

a computing unit that performs computation based on one or more instructions obtained from an instruction region in main memory (Fig. 1, element 22), and

an. instruction sequence reuse window unit that determines instruction sequence dependency relationship information and produces instruction sequence I/O group data sets for prospective reuse by the computing unit (Fig. 1, element 24 and col. 2, lines 20-35), wherein the instruction sequence reuse window unit includes a dependency relation information storage memory comprising a two-dimensional (2D) matrix-arranged array of memory elements (see Fig. 2, 'reuse circuitry'; see also col. 6, lines 13-39);

Sodani shows an instruction region/sequence storage section distinct from the main memory (see Fig. 2, where element 28 and 30 is distinct from element 12 'memory' of Fig. 1). Sodani show that the reuse memory is content addressable and the load reuse memory uses addresses to search content which is similar to a CAM and RAM. However, since Sodani did not explicitly recite CAM and RAM, the examiner introduced a secondary reference (Crick) that explicitly shows CAM and RAM distinct from the main memory (see Crick, Fig. 1, element 60 'main memory' and element 30 of Fig. 2 'CAM and RAM'), for the purpose of improving performance of the memory system and thus efficiently executing instructions.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Crick in the invention of Sodani of using the reuse memory and load reuse memory of Sodani as CAM and RAM

memories to forming a reuse table for storing and retrieving I/O group data sets, for the purpose of utilizing instructions that have been executed and reusing them which significantly improves performance.

Allowable Subject Matter

15. Claim 1-29 are allowable over prior art on record.

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Response to Arguments

16. Applicant's arguments with respect to claim 32 have been considered but are moot in view of the new ground of rejection.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/IDRISS N ALROBAYE/
Primary Examiner, Art Unit 2183